





Sn63Pb

Sn63Pb

Sn42Bi

Sn42Bi

Sn63Pb

Sn63Pb

Sn42Bi

Sn42Bi

Sn63Pb

50

50

50

50

125

125

125

125

50

Set 1 TV configurations

6

6

M5 A2

M5 B2

M6 A1

M6 B1

M9 A2

M9 B2

M10 A1

M10 B1

Phase 1

# Reliability Analysis and Finite Element Modeling of a Flexible Hybrid Electronic Device Varun Soman<sup>1</sup>, Mark D. Poliks<sup>1</sup>, James N. Turner<sup>1</sup>, Mark Schadt<sup>2</sup>, Frank Egitto<sup>2</sup>, Michael Shay<sup>2</sup> 1. State University of New York at Binghamton 2. i3 Electronics Inc.

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Ju 10

ith

No.

20

18

Defects 16

12 Nith

Joints

of

No.

10

## Set 2 TVs

• Substrate: 50 µm thick Kapton<sup>®</sup> PI.

• Electrical circuit: 2 μm thick

 Solder: Sn63Pb (reflow temp: 205 °C) or Sn42Bi (reflow temp: 175 °C). Improved solder pad design.



Original (left) and improved (right) solder pad design

## **Bend Testing Procedure:**

1. Microscopy and imaging of 20 solder joint locations of AD8232 chip to documents manufacturing defects.

2. 1000 bend cycles on 4'' - 0.5'' radius mandrels. 3. Microscopy and imaging after each stage to study and document new defects/failures.



Mandrel pushing against sensor side

### **Results:**



Defect due to crack initiation/local delamination





![](_page_0_Figure_23.jpeg)

Pad	Cu	<b>PI Thickness</b>
gn	Thickness (µm)	(µm)
nal	2	50
nal	6	50
nal	2	125
ved	2	50
ved	6	50